



CE-ATA Technical Errata

Errata ID	Protocol 004
Affected Spec Ver.	Protocol 1.0
Corrected Spec Ver.	

Submission info

Name	Company	Date
Amber Huffman	Intel	04/18/2005

Description of the specification technical flaw (add space as needed)

The time between the R1(b) response for RW_MULTIPLE_BLOCK (CMD61) and the command completion signal disable signal is incorrect. The required time between these two tokens is N_{RC} cycles, not N_{CR} cycles as specified. This errata updates the text and figure to reflect this requirement, and includes the definition for N_{RC} in the timing specifications since it was not previously used.

Description of the correction

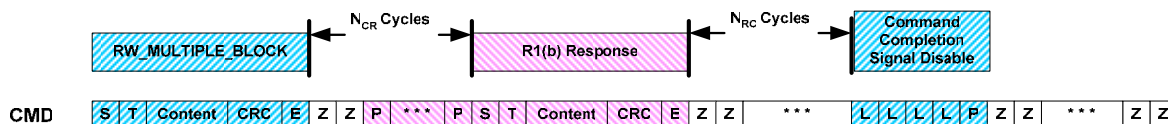
Add the following definition for N_{RC} to the table at the beginning of section 3:

N_{RC}	Number of cycles between the end bit of the response token and the start bit of the next MMC command token. See the MMC reference.
----------	--

Add the following paragraph immediately prior to Figure 15 in section 3.2.6:

The host shall not transmit the command completion signal disable to the device until N_{RC} cycles after the end bit of the R1(b) response for RW_MULTIPLE_BLOCK (CMD61) is received, as shown in Figure 15.

Update Figure 15 in section 3.2.6 with the figure below. Specifically, N_{CR} cycles between R1(b) Response and Command Completion Signal Disable is changed to N_{RC} cycles and “R1 Response” is changed to “R1(b) Response”.



Disposition log

04/18/2005	Erratum captured
06/17/2005	Erratum ratified

Technical input submitted to the CE-ATA Workgroup is subject to the terms of the CE-ATA contributor's agreement.